

| L Number | Hits | Search Text   | DB  | Time stamp          |
|----------|------|---|---|---------------------|
| -        | 1    | (shadow adj (rom or memory or bios)) and "1394" and "1212"  | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>11:21 |
| -        | 0    | 6640312.URPN.   | USPAT   | 2004/10/28<br>10:58 |
| -        | 5    | ("5875313"   "5923673"   "5937175"   "5953511"   "6389560"   "2001/0044914"   "2002/0049933").PN. | USPAT   | 2004/10/28<br>10:58 |
| -        | 3    | (shadow adj (rom or memory or bios)) and "1394"   | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>11:01 |
| -        | 2    | (shadow adj (rom or memory or bios)) and firewire   | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>11:01 |
| -        | 1    | shadow near6 (config\$10 adj rom)   | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>11:23 |
| -        | 93   | shadow near6 (config\$10 near10 (memory or bios or rom))  | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>11:23 |
| -        | 0    | (shadow near6 (config\$10 near10 (memory or bios or rom))) and "1394" and "1212"                  | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>11:23 |
| -        | 4    | (shadow near6 (config\$10 near10 (memory or bios or rom))) and "1394"                             | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>11:33 |
| -        | 5    | (shadow near6 (config\$10 near10 (memory or bios or rom))) and "1212"                             | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>12:20 |
| -        | 72   | "1212" and "configuration rom"  | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>12:21 |
| -        | 65   | ("1212" and "configuration rom") and "1394"   | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>13:13 |
| -        | 0    | ((("1212" and "configuration rom") and "1394") and shadow   | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>12:24 |
| -        | 22   | ("1212" and "configuration memory") and "1394"  | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>13:14 |
| -        | 428  | shadow adj (rom or memory or bios)  | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>14:14 |

|   |      |  |   |                     |
|---|------|--|---|---------------------|
| - | 22   | (shadow adj (rom or memory or bios)) and "1212"                | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/10/28<br>14:17 |
| - | 1    | (shadow adj (rom or memory or bios)) and (ieee near5 "1212")   | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/10/28<br>14:14 |
| - | 3    | (shadow adj (rom or memory or bios)) and "1394"                | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/10/28<br>14:21 |
| - | 33   | shadowing and "1394" and "1212"                                | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/10/28<br>14:28 |
| - | 1    | ("6553432").PN.  | USPAT;<br>US-PGPUB                                      | 2004/10/28<br>14:28 |
| - | 0    | ((("6553432").PN.) and "1394" and shadow and "1212"            | USPAT;<br>US-PGPUB                                      | 2004/10/28<br>14:32 |
| - | 28   | shadow\$10 and bios and "1394" and "1212"                      | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/10/28<br>14:33 |
| - | 282  | csr and "1394"   | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/10/28<br>17:13 |
| - | 6    | (csr and "1394") and shadow\$10                                | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/10/28<br>17:13 |
| - | 113  | "13213" and "1394"   | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/10/29<br>08:26 |
| - | 1    | ("13213" and "1394") and shadow\$10                            | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/10/29<br>10:51 |
| - | 3812 | (710/100,305-306,313-315,104).CCLS.                            | USPAT;<br>US-PGPUB                                      | 2004/10/29<br>10:52 |
| - | 333  | ((710/100,305-306,313-315,104).CCLS.) and ("1394")             | USPAT;<br>US-PGPUB                                      | 2004/10/29<br>10:52 |
| - | 13   | ((710/100,305-306,313-315,104).CCLS.) and ("1394")) and shadow | USPAT;<br>US-PGPUB                                      | 2004/10/29<br>10:53 |

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 1394 and 1212 and ("shadow  
 bios" or "shadow rom"  
 or "shadow memory")

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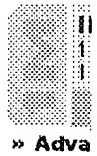
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 configuration and ("shared  
memory" or "shared bios"  
or "shared rom") and (1394 or  
1212)

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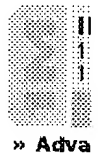
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- 3) Limit the results by selecting Search Options.
- 4) Click Search. See [Search Examples](#)

 configuration and ("shared  
memory" or "shared bios"  
or "shared rom")

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1394 and 1212 and ("shadow bios" or "shadow rom" or "shado



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### 1 [Boosting superpage utilization with the shadow memory and the partial-subblock TLB](#)



Cheol Ho Park, JaeWoong Chung, Byeong Hag Seong, YangWoo Roh, Daeyeon Park

 May 2000 **Proceedings of the 14th international conference on Supercomputing**

 Full text available: pdf(798.29 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

While superpage is an efficient solution to increase TLB reach, its limited flexibility for address mapping is still a hard issue. Our proposed mechanism has been developed for taking advantage of two previous approaches which resolve the issue partially: the partial-subblock TLB and the shadow memory. Through integration of them, our mechanism enjoys various benefits inherited from the both sides. By adopting Memory Controller TLB (MTLB) from the shadow memory, it allows superpages to be c ...

### 2 [Increasing TLB reach using superpages backed by shadow memory](#)



Mark Swanson, Leigh Stoller, John Carter

 April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3

 Full text available: pdf(1.32 MB) [Publisher Site](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The amount of memory that can be accessed without causing a TLB fault, the reach of a TLB, is failing to keep pace with the increasingly large working sets of applications. We propose to extend TLB reach via a novel Memory Controller TLB (MTLB) that lets us aggressively create superpages from non-contiguous, unaligned regions of physical memory. This flexibility increases the OS's ability to use superpages on arbitrary application data. The MTLB supports shadow pages, regions of physical address ...

### 3 [An architectural framework for migration from CISC to higher performance platforms](#)



Gabriel M. Silberman, Kemal Ebcioglu

 August 1992 **Proceedings of the 6th international conference on Supercomputing**

 Full text available: pdf(2.04 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We describe a novel architectural framework that allows software applications written for a given Complex Instruction Set Computer (CISC) to migrate to a different, higher performance architecture, without a significant investment on the part of the application user or developer. The framework provides a hardware mechanism for seamless switching between two instruction sets, resulting in a machine that enhances application performance while keeping the same program behavior (from a user per ...